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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,575	03/25/2004	Kuniyuki Tani	65933-081	5532
7:	590 02/15/2006		EXAMINER	
McDERMOTT, WILL & EMERY			CUNNINGHAM, TERRY D	
600 13th Street Washington, D	, N.W. OC 20005-3096		ART UNIT	PAPER NUMBER
•			2816	
			DATE MAILED: 02/15/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)				
		10/808,575	TANI ET AL.	(AV)			
Office Ac	tion Summary	Examiner	Art Unit				
		Terry D. Cunningham	2816				
The MAILING Period for Reply	DATE of this communication app	pears on the cover sheet with the	correspondence add	dress			
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
2a) ☐ This action is F 3) ☐ Since this appli	cation is in condition for allowa	ecember 2005. s action is non-final. nce except for formal matters, pro Ex parte Quayle, 1935 C.D. 11, 4		merits is			
Disposition of Claims							
4) Claim(s) 1-21 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 1-4,9,11-13,18,20 and 21 is/are rejected. 7) Claim(s) 5-8,10,14-17 and 19 is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. Application Papers							
_							
9) The specification is objected to by the Examiner. 10) The drawing(s) filed on <u>25 March 2004</u> is/are: a) accepted or b) objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C.	& 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.							
Attachment(s)							
1) X Notice of References Cit		4) Interview Summary					
	Patent Drawing Review (PTO-948) tatement(s) (PTO-1449 or PTO/SB/08) 02/06	Paper No(s)/Mail D 5) Notice of Informal F 6) Other:		-152)			

DETAILED ACTION

Reopen Prosecution

This paper is in response to the Appeal Brief filed 30 December 2005. Prosecution on the merits is hereby reopened for the purposes of ensuring that all the requirements for Appeal are met and for introducing new grounds of rejection and new points of arguments.

Summary of changes in this action

- 1. Examiner has found Applicant's remarks concerning claims 5, 7 and 14 persuasive. As seen, the applied reference does not include the "CMOS transistor" and two "switching elements". Thus, the rejection to claims 5, 7 and 14 is hereby removed.
- 2. New objections and indefiniteness rejections are included.

Claim Objections

Claim 1 is objected to because "-1", in line 1, should be changed to --1--. Appropriate correction is required

Claim Rejections - 35 USC § 112

Claims 5, 6, 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, line 9, "a switching element" has already been recited in line 7. It is suggested that the claim be amended to recite --a first switching element-- and --a second switching element--.

Claim 6 is indefinite for similar reason as claim 5. Also, in line 2, it is not understood how one "transistor" can comprise two transistors. Similar to claim 5, it is suggested that "CMOS transistor" be changed to --CMOS transistor pair--.

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Claim 14 is indefinite for similar reason as claim 5.

Claim 15 is indefinite for similar reason as claim 6.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Curd (USPN 5,650,672). Curd discloses, in Fig. 1, a circuit comprising: "a driving unit (circuit of Fig. 1, less the circuit generating IN0X and IN1X and 414) which generates a bias voltage (VPI) to be applied to a predetermined load (receiving VPI)", the "driving unit" including" a plurality of bias circuits (N1 and P1) which are connected in parallel and have different current driving capabilities"; and a control unit (the circuit generating IN0X and IN1X and 414) which switches a current driving capability of the driving unit according to a variation in an amount of current required for the load (as determined by IN0X and IN1X) in a period for applying the bias voltage to the load.

Claims 1, 3, 4 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Herndon (USPN 5,506,541). Herndon discloses, in Fig. 4, a circuit comprising: "a driving unit (circuit of Fig. 4, less the circuit generating PC(0)-PC(3)) which generates a bias voltage (VRRG) to be applied to a predetermined load (receiving VRRG)", the "driving unit" including" a plurality of bias circuits (117-120) which are connected in parallel and have the same current driving capability"; and a control unit (the circuit generating PC(0)-PC(3)) which switches a current

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driving capability of the driving unit according to a variation in an amount of current required for the load (as determined by PC(0)-PC(3)) in a period for applying the bias voltage to the load.

Reference is made to line 59-61 of Col. 6 of Herndon which states that elements 117-120 can be the same size, thus having the "same current driving capabilities".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11, 12, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Signell et al. (USPN 6,028,546) in view of Curd (USPN 5,650,672). Signell et al. disclose, in Fig. 4, a pipeline analog-to-digital conversion comprising: "an amplifier unit (32-4) which repeats and auto-zero operation and an amplification operation alternately" and "bias voltage generating circuit (not show, but disclosed as biasing the circuit of Fig. 4)". However, the reference to Signell et al. does not expressly disclose details for the "bias voltage generating circuit". The above discussed "bias voltage generating circuit" to Curd is disclosed as having the advantage of provide efficient dual-mode operation allowing for power savings. Therefore, it would have been obvious for one skilled in the art to use the specific "bias voltage generating circuit" of Curd for the broadly disclosed "bias voltage generating circuit" of Signell et al. to obtain the expected advantage of efficient dual-mode operation allowing for power savings.

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Claims 11, 13, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Signell et al. (USPN 6,028,546) in view of Herndon (USPN 5,506,541). Signell et al. disclose, in Fig. 4, a pipeline analog-to-digital conversion comprising: "an amplifier unit (32-4) which repeats and auto-zero operation and an amplification operation alternately" and "bias voltage generating circuit (not show, but disclosed as biasing the circuit of Fig. 4)". However, the reference to Signell et al. does not expressly disclose details for the "bias voltage generating circuit". The above discussed "bias voltage generating circuit" to Herndon is disclosed as having digitally controlled variable output voltage. Therefore, it would have been obvious for one skilled in the art to use the specific "bias voltage generating circuit" of Herndon for the broadly disclosed "bias voltage generating circuit" of Signell et al. to obtain the expected advantage of providing a digitally controlled variable output voltage.

Claims 5-8, 10, 14-17 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Examiner has fully considered Applicant's remarks for the above art rejections and has not found them to be persuasive. As modified, it is seen that the rejection in view of Herndon meets the claim language. Also, newly cited reference to Herndon discloses "bias circuit" having "the same current driving capability" for claims 3 and 13.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terry Cunningham whose telephone number is 571-272-1742. The examiner can normally be reached on Monday-Thursday from 7:30 to 6:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TC February 8, 2006 Terry D/Cunninghar Primary Examiner Art Unit 2816